Trends in the design of front-end systems for room temperature solid state detectors

Pier Francesco Manfredi and Valerio Re

Abstract-- **The paper discusses the present trends in the design of low-noise front-end systems for room temperature semiconductor detectors. The technological advancement provided by submicron CMOS and BiCMOS processes is examined from several points of view. The noise performances are a fundamental issue in most detector applications and suitable attention is devoted to them for the purpose of judging whether or not the present processes supersede the solutions featuring a field-effect transistor as a front-end element. However, other considerations are also important in judging how well a monolithic technology suits the front-end design. Among them, the way a technology lends itself to the realization of additional functions, for instance, the charge reset in a charge-sensitive loop or the time-variant filters featuring the special weighting functions that may be requested in some applications of CdTe or CZT detectors.**

Index Terms —**Front-end electronics, MOSFET, Noise, JFET**

I. Introduction

For a better understanding of the present trends in the design of front-end systems for room temperature detectors, it is useful to review how the front-end concepts have evolved during the past twenty years. The advent of the first vertex detectors for collider-type accelerators in particle physics made it clear that a front-end based on a monolithic approach was the only way to solve the problem of extracting and processing the signals from the high-density configurations of electrodes [1, 2]. At the same time the diffusion of imaging techniques in highly diversified fields was setting the request for even more finely segmented detectors, also needing high density multichannel signal processors.

In either case, the front-end circuits are mixed-signal architectures combining an analog section and a logic section with a generally high functional density. Understandably, the first readout chips for segmented detectors relied upon CMOS as a readily available technology.

It became clear soon, however, that the CMOS processes of that time, featuring a gate length of a few microns and a thickness of the gate oxide of some tens of nanometers did not suit the most demanding applications. Noise was a serious limitation. The 1/f noise associated with the channel current brought about a substantial contribution to the total equivalent noise charge ENC. Secondly, those CMOS processes were not radiation resistant to the extent required in several applications.

The noise issue conveyed the attention on monolithic processes featuring, along with the complementary MOSFETs devices, like a junction field-effect transistors (JFET) or a bipolar transistors, outperforming the MOSFETs from the noise standpoint.

Technologies like JFET-CMOS (Fraunhofer, Max Planck Institut, Pavia) and Bi-JFET-CMOS (DMILL) were developed and employed in some applications [3, 4]. They are still available and may be useful in some particular situations. The same technologies also provided an upgraded radiation hardness as compared to the CMOS processes of the older generations. DMILL was conceived to be intrinsically radiation hard. The JFET-CMOS process would lend itself to a radhard design by a judicious circuit conception. It was recognized, indeed, that in the older CMOS processes, the most radiation-sensitive device was the N-MOS, so a design entirely based on N-JFET and P-MOS proved to lead to suitably radhard chips [5].

New trends in the front-end design have appeared as a consequence of the advancement in CMOS processes known as *device scaling*. The device scaling has considerably reduced the gate length, entering the submicron and deep submicron regions, by virtue of which devices with gate length down to 0.1 μm are nowadays available. Perhaps even more importantly, it acted also in the sense of reducing the thickness of the gate oxide to a few nanometers. The result of a shorter gate and a thinner gate oxide is a remarkable improvement in noise and radiation hardness features of the CMOS processes, such to make them fully adequate for front-end design [6, 7].

It is obvious to wonder where we stand now with the front-end design, as the upgraded CMOS processes are confining the JFET to a few, though scientifically relevant applications

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and new achievements, like CMOS processes featuring a Si-Ge bipolar transistor are appearing on the scene.

II. Relative Merits Of JFETs And Submicron MOSFETs As Front-End Devices

The discussion on the relative merits of JFETs and MOSFETs as front-end devices in a low-noise charge-sensitive loop must be done on the basis of two aspects. One is the intrinsic noise behavior of either device. The second one is how suitable they are to implement an important function in the charge-sensitive loop, which is the charge reset of the integrating capacitor optimized from the noise standpoint.

As far as the intrinsic noise behavior goes, the reduction in the gate oxide thickness t_{ox} to the few nanometer region has produced a considerable reduction of 1/f-noise in the submicron CMOS families. The 1/f-noise has attained acceptably low values in the P- MOSFET, although in terms of absolute improvement the effect on the N- MOSFET has been quantitatively more evident. A thinner gate oxide and a shrinking in the gate length have also upgraded the behavior of the high frequency noise (frequency independent or white) at reasonably small standing currents. While a JFET still has a better noise behavior at very low frequencies, it is outperformed by a submicron channel MOSFET at high frequencies. To confirm these considerations, a comparison is done on two devices, an N-channel JFET and a P-channel MOSFET that are close to the technological frontier in their relevant categories. Both devices, that are parts of monolithic processes, have a gate width W = 2000 μm. The N-channel JFET belongs to the Fraunhofer JFET-CMOS process. It has a gate length of 1.2 μm and is set to work at a 500 μA drain current. Its voltage noise spectral density is plotted as a function of frequency in Fig. 1a). The P-channel MOSFET belongs to a process of 0.35 μm minimum gate length and 7.2 nm gate oxide thickness. Set to work at a standing current of 250 μA, it features the voltage noise spectral density plotted as a function of frequency in Fig. 1b) [8].

The extent to which the submicron channel P-MOS outperforms the JFET in terms of high frequency noise is apparent from Figs. 1 a) and b). The JFET has been set to operate at a current which is twice as much that of the MOSFET to partially offset the difference in channel lengths. In spite of this, the noise voltage spectrum of high-frequency noise in the N-JFET is about 2 $nV/(Hz)^{1/2}$, against the 1.3 $nV/(Hz)^{1/2}$ of the P-MOS. The advantage of the PMOS from the standpoint of the high frequency noise becomes even more evident when a low-noise application is subject to constraints on power dissipations. In what follows, it will be assumed that the high frequency noise is basically the channel thermal noise. This assumption is very reasonable for the actual JFET, which has a gate length of more than 1 μm, while for the deep submicron MOSFETs it may be true only as a first approximation, because short channel effects may be present.

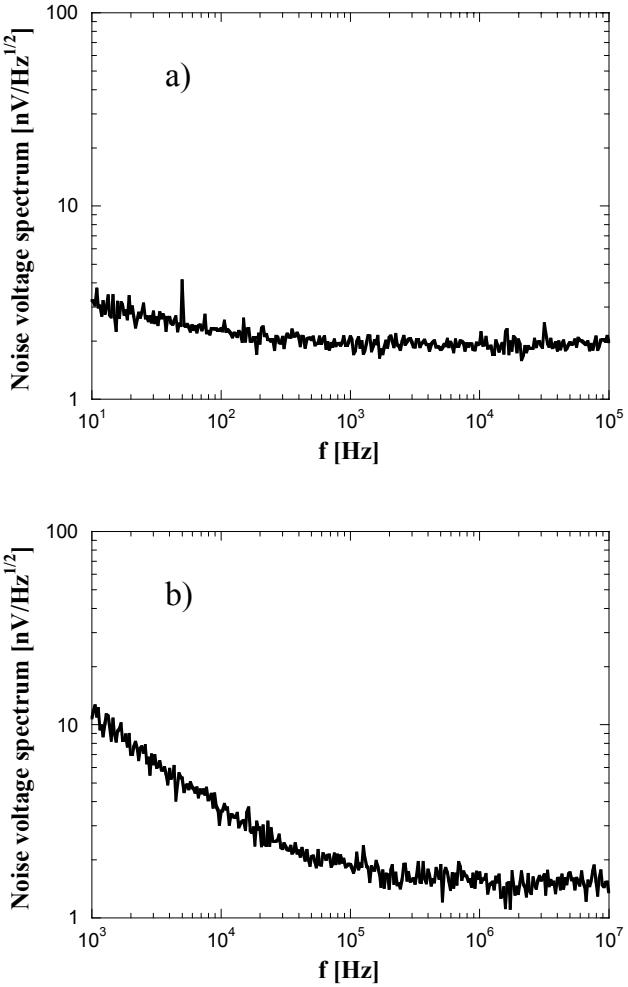

Fig. 1. Comparison of the noise voltage spectral densities of a JFET and a submicron MOSFET of equal gate width W = 2000 μm.
a): N-JFET of 1.2 μm gate length operating at a drain current of 500 μA;
b): P-MOS of 0.35 μm gate length operating at a drain current of 250 μA.

The noise spectra of Fig. 1 can be described on the basis of a constant spectral power density S_w, whose square root is the asymptotic value at $f \rightarrow \infty$ in the plots of Fig. 1, and by a spectral power density

$$S_{1/f}(f) = \frac{A_f}{f} \qquad (1)$$

which is related to the behavior of the noise spectra at low frequencies. Strictly speaking, the 1/f-noise provides an accurate description of low-frequency noise in a MOSFET. The low-frequency noise mechanism in a JFET is different. However, as the noise spectra of Fig. 1 show that also in the JFET the low-frequency noise is governed by a 1/f law, both cases will be represented by the same type of low-frequency noise behavior. By multiplying A_f by the device capacitance C_i, the product $H_f = C_i A_f$ is obtained, which is the intrinsic coefficient of 1/f-noise, independent of the gate width W of

the device [9]. In a MOSFET, for a specified type of charge carrier, H_f is proportional to the thickness t_{ox} of the gate oxide and depends on the nature of the oxide.

In the case of a frequency-independent noise determined exclusively by the channel thermal noise, S_w would be represented by the relationship:

$$S_W = 4kT\frac{\Gamma}{g_m} \tag{2}$$

where k is Boltzmann's constant, T the absolute temperature, g_m the transconductance and Γ the coefficient of the channel thermal noise. The value of Γ is close to unity, although it may be substantially different for the JFET and the MOSFET.

If the devices described by the noise spectra of Fig. 1 a) and b) were employed as front-end elements of a charge-sensitive preamplifier, followed by a shaper of peaking time t_p, their spectral densities would reflect into the ENC contributions that are plotted in Fig. 2 as functions of the peaking time t_p.

The ENC values have been obtained by introducing the values of S_w and A_f evaluated from Fig. 1 into the equation:

$$ENC^2 = \left(C_D^* + C_i\right)^2\left(\frac{S_W A_1}{t_P} + 2\pi A_f A_2\right) \tag{3}$$

where C_D* is the total external capacitance at the preamplifer input, and C_i is the device input capacitance. A_1 and A_2 are coefficients of the shaper for the two types of noise [10]. For the sake of reference, the shaper is assumed to provide a piecewise quadratic shape whose noise coefficients are $A_1 = 1.33$ and $A_2 = 0.57$.

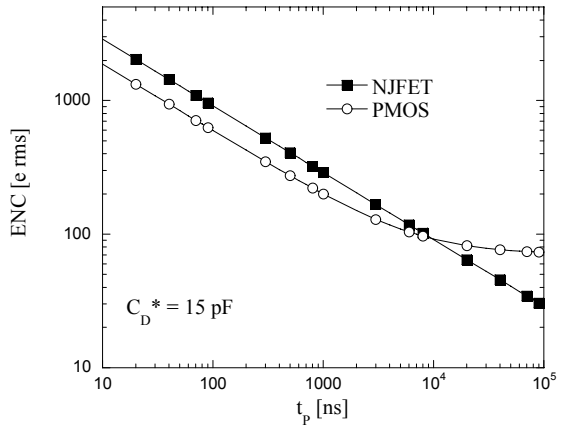

Fig. 2. Contributions to ENC evaluated from the spectra of Fig. 1, as functions of the peaking time t_p.

The presence of a larger amount of 1/f-noise in the P-MOS is responsible for the leveling-off in the ENC vs t_p curve of Fig. 2, which is unnoticeable for the JFET in the explored range of t_p values. As Fig. 2 shows, there is a crossover t_p value beyond which the JFET provides smaller ENC values. In the case of the devices compared in Fig. 2 such value of t_p is about 8 μs. It has been found that the values of the coefficient A_f which describes the spectral power density $S_w = A_f/f$ of the 1/f-noise in P- MOSFETS, as t_{ox} is varied, barely spans a one decade range, 10^{-13} V^2 < A_f <10^{-12} V^2 for devices of W=2000μm. The resulting values of the crossover peaking time t_p are plotted in Fig. 3.

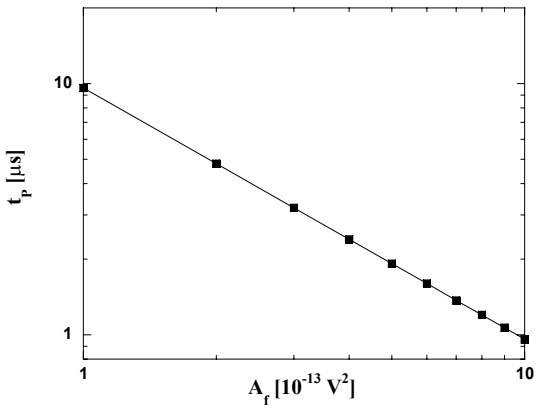

Fig. 3. Value of peaking time t_p at which the ENC contributions of voltage noise for the N- JFET and the P-MOS become equal, plotted as a functions of the A_f coefficient of the P-MOS.

The curve of Fig. 3 points out that the deep submicron P-MOS, by virtue of the noise improvement related to the device scaling has restricted the boundary of the region of peaking times where the JFET offer superior noise performances to 1 μs or more. For a particularly good specimen like the P-MOS of Figs. 1 and 2, this region may begin farther on, at a value close to 10 μs. These considerations underline an important aspect, which partly explains the present trends in front-end design. The improvement in the CMOS noise behavior made possible by device scaling has not been accompanied by a *comparable improvement in the JFET thermal noise*.

However, the JFET cannot be considered to be totally superseded by the CMOS in low-noise applications for the following reasons. First, the low-frequency noise behavior of the JFET is so good that a leveling-off in the ENC vs t_p dependence is not perceivable in the range of t_p values employed in most applications. Which means that, in a preamplifier utilizing a nonresistive charge reset to minimize the parallel noise contribution, ENC keeps decreasing as t_p is increased up to extremely long values. This feature is enforced by the fact that the JFET offers intrinsically better option than the MOSFET in the realization of the charge reset in the charge-sensitive loop. Viable solutions with a MOSFET front-end are an extremely large MOS resistor, a MOS switch in parallel to the feedback capacitance or a transconductor operating at an extremely small standing current, down to a fraction of a pA [10, 11, 12]. All these

solutions, however, add a capacitive contribution at the preamplifier input. The JFET offers solutions that are exempt from this limitation. Among them the charge reset based on the forward biased gate-to-source junction or the one actuated by drain feedback, which can be designed to operate in either continuous or pulsed mode [13, 14, 15].

Another important aspect of the JFET solution is the classical JFET technology, where the channel resides in an epitaxial layer and topside and backside gates are obtained by diffusion and connected together to implement the so called triode configuration, which makes the device free from thermal noise contributions arising from the backside gate. This is a very well established technology, which has been employed for decades in the fabrication of low-noise discrete JFETs. Devices based on this process, besides featuring a very small low-frequency noise, have a very well predictable channel thermal noise which follows the relationship (2) with Γ close to the value of 0.7 predicted by the theory for a long channel device.

A successful attempt to transfer the characteristics of the classical JFET process into a monolithic technology was carried out as a joint effort by Brookhaven National Laboratory, Interfet Corporation and Pavia University [16, 17]. The integration process is based upon a buried layer approach, where the individual JFETs are realized on insulated P+ islands that become the backside gates of the JFETs. The process provides the compatibility of several top quality N-channel JFETs on the same substrate. The integrated JFETs were proven to retain the features of the corresponding discrete parts. This technology is restricted in its application to the preamplifier section of the front-end and, as such, it must be completed by a separate CMOS chip for all further functions.

An example of a monolithic JFET preamplifier obtained with the buried layer process is shown in Fig. 4. The circuit of Fig. 4 employs the nonresistive charge reset based on the principle of the forward biased gate-to-source junction.

In the circuit of Fig. 4, J_1 and J_2 realize the input cascode, while J_3, J_4, J_7 provide a high impedance load on the drain of J_2 and J_8 is the output buffer. The ENC vs t_p dependence of Fig. 5 shows the constant decrease in ENC at increasing t_p, a demonstration of the outstanding noise behavior of the preamplifier in the low-frequency region.

Two series of monolithic preamplifiers differing for the size of J_1 and suiting two different detector applications, namely calorimetry and spectrometry with large Ge detectors, have been realized on the basis of the buried layer approach. Both series are still in production.

As a confirmation of the reproducibility of the noise behavior of preamplifiers obtained with the buried-layer process, Fig. 6 shows the frequency distribution of the ENC values measured on a set of 210 monolithic preamplifiers [18].

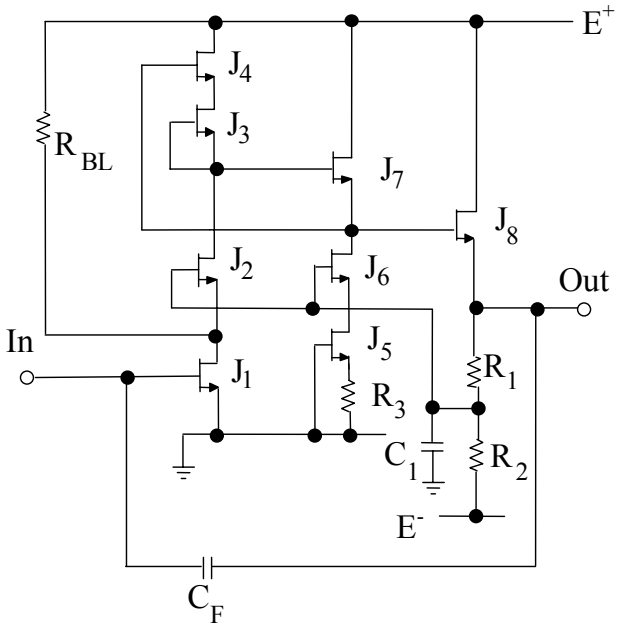

Fig. 4. Monolithic charge-sensitive preamplifier employing a nonresistive charge reset.

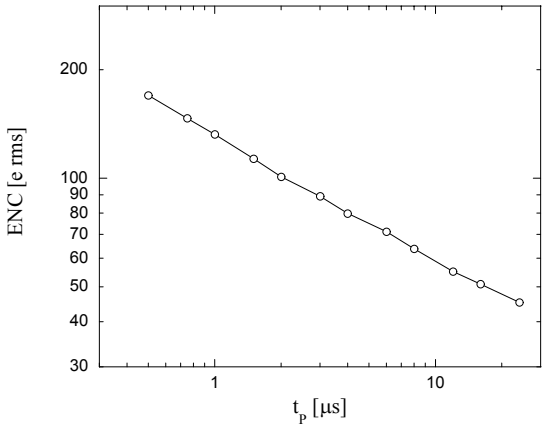

Fig. 5. ENC as a function of t_p at zero detector capacitance for the charge-sensitive preamplifier with nonresistive charge reset of Fig. 4.

A final interesting point about JFETs as front-end devices is the choice between N and P-channel. In most of applications the choice would favor the N-channel because of the higher mobility of its majority carriers. However, there is one case where the use of the P-channel would, instead, be advisable. This is the case of devices exposed to irradiation. It has been shown in the case of exposure to gamma rays that the characteristic frequencies of Lorentzian noise, that are responsible for a consistent increase of ENC in the irradiated devices occur at a much lower frequency in the P-channel than in the N-channel device [19]. Therefore, although the P-device has a larger channel thermal noise before and after irradiation, there is broad frequency range where the

irradiated P-device features less noise than the irradiated N-device, as apparent in Fig. 6.

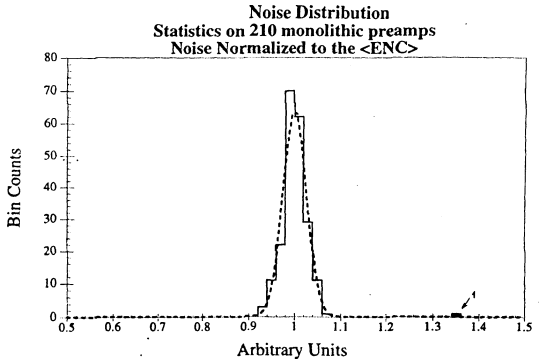

Fig. 6. Frequency distribution of the ENC values obtained on a set of 210 samples of monolithic preamplifiers based on the buried-layer approach.

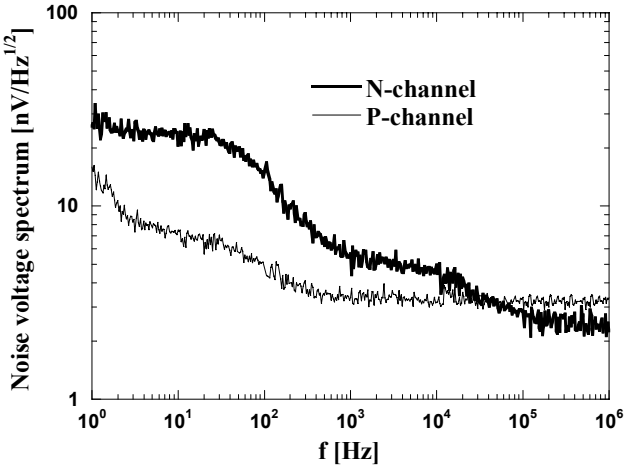

Fig. 7. Spectral density of voltage noise in P and N-channel JFETs exposed to ^{60}Co γ-rays at a total dose of 1 Mrad. The devices, both with W/L = 800/4, were operated at 0.8 mA.

III. JFET Preamplifiers On High Resistivity Silicon

The line of research aiming at realizing active devices on high resistivity silicon began when the advent of the solid-state drift chamber, featuring an extremely small capacitance of its output electrode set the requirement that such capacitance be increased to a negligible extent by the front-end device [20, 21]. The present realization of a charge-sensitive preamplifier on a detector grade, high resistivity substrate serves a different purpose. It addresses the problem of extracting and processing the signals in a microstrip detector with preamplifiers integrated on the detector chip in order to avoid decoupling capacitors, a cumbersome aspect in double-sided microstrip detectors, and to simplify the connections to the external world [22]. For this purpose, the preamplifier architecture of fig. 4 has been transferred on a high resistivity substrate. The input device has a gate width W = 1000 μm and a gate length L = 4 μm. Among the available options, there is one with a nonresistive charge reset based on the principle of the forward biased gate-to-source junction.

The ENC vs t_p curve is given in Fig.7 for the case of nonresistive charge reset. The ENC behavior is similar to that of Fig. 5, which points out that also the version on high resistivity silicon has a good noise behavior in the low frequency region. However, the comparison of theoretical predictions and experimental data show that the contribution from channel thermal noise is larger than expected. This has been attributed to a thermal noise contribution from the back gate of the input device.

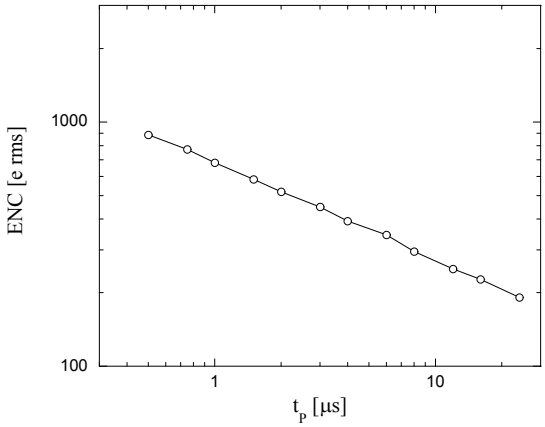

Fig. 8. ENC for a preamplifier with nonresistive charge reset fabricated in high resistivity silicon at a detector capacitance of 8 pF.

IV. Submicron MOSFETs As Front-End Devices

Having pointed out in section II that the device scaling in CMOS processes and the resulting noise improvement have considerably restricted the field of application of JFETs, it is necessary now to investigate some aspects related to the low-noise applications of submicron and deep submicron MOSFETs. A first set of useful information is provided by a thorough investigation done on two CMOS processes produced by the same foundry, STMicroelectronics. One of them, called 6G has a minimum gate length L_{MIN} of 0.35 μm and a gate oxide thickness t_{ox} = 7.2 nm. The second one, called H8D, has a minimum gate length L_{MIN} of 0.18 μm and a gate oxide thickness t_{ox} = 4 nm [8, 23].

The spectral densities of the noise voltage of N and P-channel MOSFETs belonging to the process of 0.18 μm minimum gate length are plotted in Fig. 9. Both devices have a gate width W = 2000 μm and a gate length of 0.35 μm. It must not be surprising that the devices have been designed with a gate length longer than the minimum one allowed by the technology. This is related to the experimentally observed

fact that in the deep submicron region, devices featuring the minimum gate length in a process may feature more low-frequency noise than devices of longer L.

As apparent from Fig. 9, the P-channel MOSFET has a considerably smaller 1/f – noise than the N-channel device, a behavior which has been known for a long time. An aspect which, instead, is somewhat surprising is that no difference is noticeable in the high frequency region of the noise spectra, where a better behavior of the N-channel device would be expected. In order to clarify this point, the transconductances of the two devices were measured. They are compared in Fig. 10 and confirm that, as expected from considerations of carrier mobility in the two devices, the transconductance at the same standing current is higher in the N-channel device. The noise behavior of Fig. 9 was observed in P and N-channel pairs of different gate lengths and belonging to both processes, L_{MIN} = 0.35 μm and L_{MIN} = 0.18 μm. Undoubtedly, if the fact that the larger g_m in the N-channel device does not reflect into a smaller channel noise at high frequencies were observed on a broader set of processes, it would deserve attention. Possible explanations for such a behavior are:

- the presence of noise related to short channel effects, like hot electrons and impact ionization noise, that are more likely to occur in the N-channel than in the P-channel device;
- a different level of inversion at the same current for the two devices, which may result in different values for the coefficient Γ in (2);
- a mere thermal noise contribution related to the layout and the nature of the process, like the thermal noise from a well.

The conclusion of the discussion about the relative merits of P and N-channel MOSFETs is that low noise design should rely almost exclusively upon the P-MOS as a front-end element. Once this decision is made, there are a few more subtle points to consider. As already pointed out, considerations of low-frequency noise suggest that devices with a gate length equal to the minimum allowed by the technology should be avoided. An example to support this consideration is provided in Fig. 11, which compares the noise spectra of three devices of equal W and equal L obtained with three processes of different minimum gate length and oxide thickness. The noise spectra of Fig. 11 show that of the three examined devices, the largest 1/f-noise occurs in the one whose gate length is the minimum length allowed by the process. That is, in the case of Fig.11 the largest 1/f-noise occurs with the process of L_{MIN} = 0.35 μm.

From a broad set of measurements of noise spectral densities done on P-MOSFETs belonging to the G6 and H8D processes it was possible to determine the contributions ENC_w and $ENC_{1/f}$ brought about to the equivalent noise charge by the frequency-independent noise and by the 1/f-noise associated with the channel current. Devices with L = 2000 μm and different gate lengths have been considered. As shown in Fig. 12, the ENC_w dependence on C_D* is almost linear and scales down regularly as the gate length is reduced.

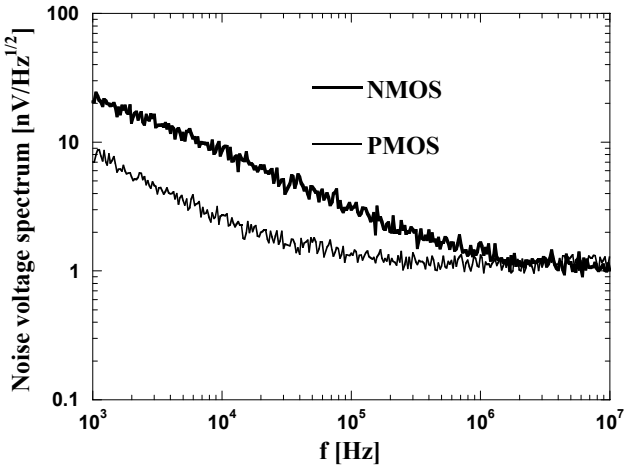

Fig. 9. Noise voltage spectra of PMOSFET and NMOSFET with W/L = 2000/0.35 belonging to the 0.18 μm process ($|V_{DS}|$= 0.8 V, V_{BS} = 0, I_D = 500 μA).

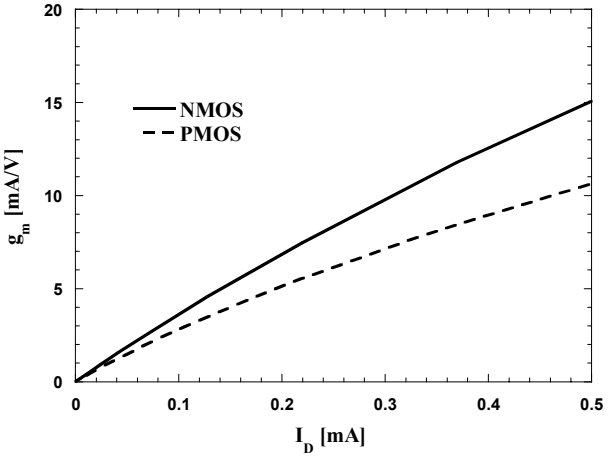

Fig. 10. Transconductance g_m as a function of the drain current I_D for NMOSFET (a) and PMOSFET (b) with W/L = 2000/0.35 belonging to a 0.18 μm CMOS process ($|V_{DS}|$ = 0.8 V, V_{BS} = 0).

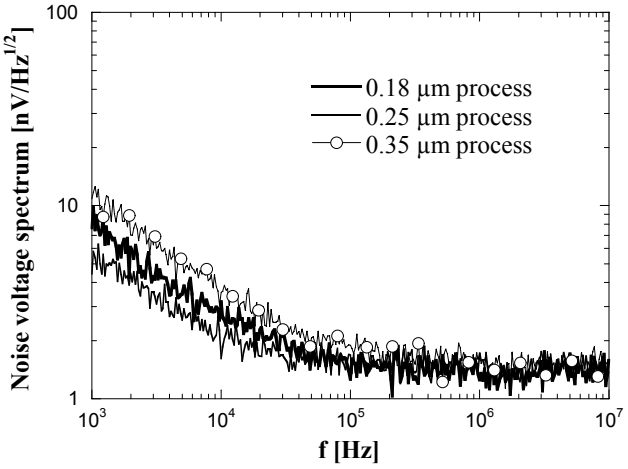

Fig. 11. Noise voltage spectra of PMOSFETs with W/L = 2000/0.35 belonging to three submicron processes (0.18 μm, 0.25 μm, 0.35 μm minimum gate length) process ($|V_{DS}|$ = 0.8 V, V_{BS} = 0, I_D = 250 μA).

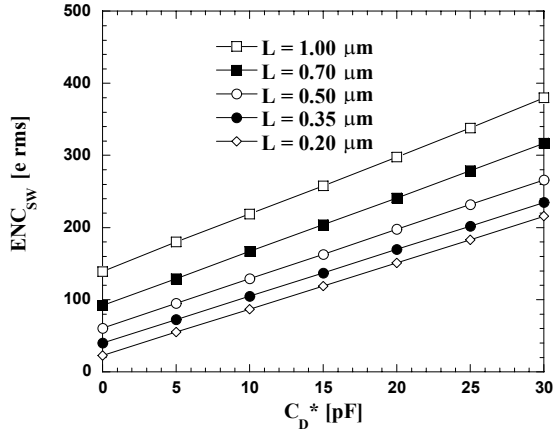

Fig. 12. ENC contribution due to the frequency-independent noise as a function of C_D* for P-MOSFETS belonging to the process with L_{min} = 0.18 μm, featuring W =2000 μm and different gate lengths.

A by far less regular behavior is observed in the $ENC_{1/f}$ dependence on C_D*, as apparent in Fig. 13.

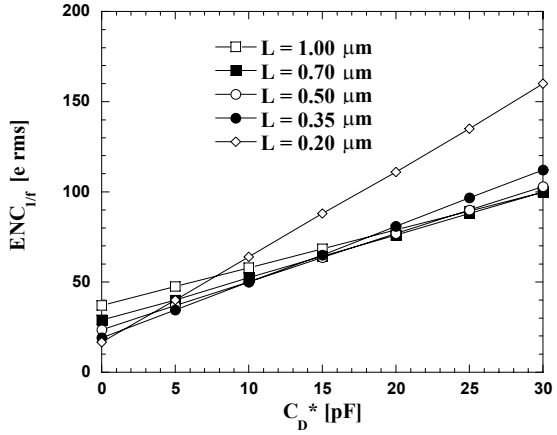

Fig. 13. ENC contribution due to the 1/f-noise as a function of C_D* for P-MOSFETs belonging to the process with L_{min} = 0.18 μm, featuring W = 2000 μm and different gate lengths.

The irregularities in the set of curves of Fig. 13 has suggested an investigation about the behavior of the intrinsic coefficient H_f of 1/f-noise on devices of different gate lengths belonging to the 6G and H8D processes. The results are plotted in Fig. 14.

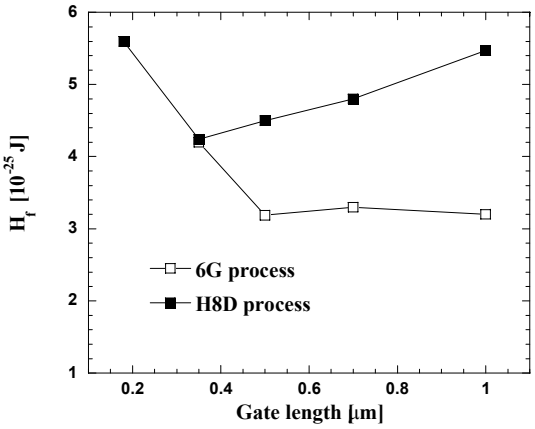

Fig.14. H_f coefficient of 1/f-noise as a function of gate length for P-MOSFETs belonging to the 6G (L_{min} = 0.35 μm) and H8D (L_{min} = 0.18 μm) processes, featuring W = 2000 μm and different gate lengths.

The plots of Fig. 14 show that for the 6G process the coefficient H_f has a larger value at the minimum gate length of the process, which is consistent with other observations on 1/f-noise. Then it remains fairly constant, as it should be, as L is increased. The devices belonging to the H8D process have a non monotonic dependence on L. Besides, in spite of the thinner gate oxide of the H8D process, it features consistently larger H_f values than the 6G process. It seems that the quality of the oxide is degraded when the thickness is reduced. It is important to call the attention on this point because any further improvement in the low-frequency noise behavior of MOSFET is strictly dependent on how well the quality of the oxide is retained in the scaling process.

Apart from the improvement in their noise performances, the *device scaling* has upgraded the behavior of MOSFETs in several other analog applications. The increase in bandwidth related to the shorter channel results in a better behavior of both time-invariant and time-variant filters realized in CMOS technology. Time-variant filters featuring a trapezoidal weighting function are of comparatively easy realization with CMOS on the basis of either current switching or a correlated double sampling approach. These weighting functions with their flat-top are useful in connection with detectors delivering signals with variations in shape, like CdTe or CZT detectors.

The realization of time-invariant filters also benefits from the increased bandwidth of CMOS. An example is provided by Fig. 15, which compares the simulated behavior of two semigaussian filters based upon the same schematic, but employing two different CMOS processes.

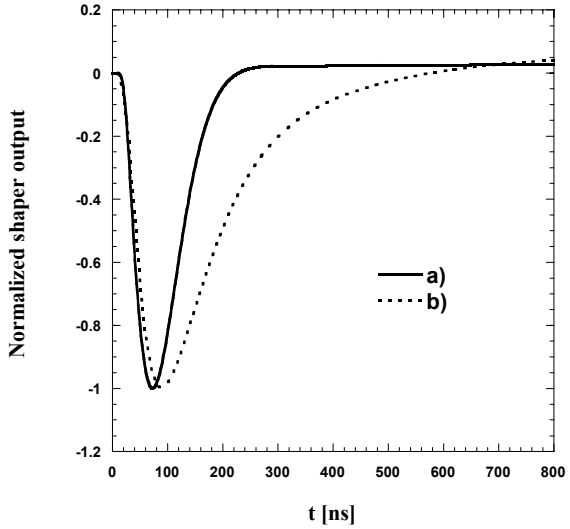

Fig. 15. Simulated shapes at the output of two semigaussian filters based on the same schematic, but on different CMOS processes: a) process with L_{min} = 0.25 μm, b) process with L_{min} = 0.8 μm.

The shape obtained with the process of shorter gate length is almost symmetric and recovers to the baseline in a very neat way. The shape obtained with the process of longer gate in nonsymmetric and longer recovery to the baseline is dictated by the need of stabilizing the shaper against a potentially oscillatory behavior related to the bandwidth limitations in the active devices.

As a final comment, being the front-end chips in general *mixed signal* circuits, it is obvious that the advantages in terms of functional density and operational speed brought about by the device scaling to the logic sections are remarkable.

V. BiCMOS Processes In The Front-End Design

The question which naturally arises in the presence of a BiCMOS technology is whether some particular low-noise situations may benefit from the availability of the bipolar transistor. In order to consider the bipolar transistor a competitor of a MOSFET, the value of the peaking time t_p must be adequately short to make the parallel noise associated with the base current of the bipolar transistor acceptable. If in a bipolar transistor only the two dominant noise sources, the shot noise in the collector current and the shot noise in the base current are taken into account, a minimum noise condition exists, expressed by:

$$I_C t_P = \frac{kT}{q}\left(C_D^* + C_i\right)\sqrt{\frac{\beta A_I}{A_3}} \qquad (4)$$

where I_C is the collector current, q is the electron charge, β is the dc base-to-collector current gain and A_3 is the filter coefficient for parallel noise, A_3 = 0.39 in the case of a piecewise quadratic shape. At a collector current of 250 μA, identical to the drain current in the MOSFET of Fig. 1, at the same detector capacitance of 15 pF and assuming β = 100, the peaking time which yields the minimum noise condition is about 30 ns. At shorter values of t_p the dominant noise contribution comes from the shot noise in the collector current. The theoretical value of the relevant voltage noise spectral density, calculated as 2kT/gm , where g_m = 10 mS at the collector current of 250 μA, would be about 0.9 nV/(Hz)$^{1/2}$. This is certainly better than the high frequency noise voltage density in the P-MOSFET of Fig. 1. To outperform the MOSFET from the standpoint of high frequency noise, however, the bipolar transistor should feature a base spreading resistance of less than 50 Ω, a value which is not so easily achieved in a bipolar transistor part of a monolithic process.

As a conclusion, the bipolar transistor might be a competitor of the short channel MOSFET provided that the two following conditions are met:

- the value of t_p is in the 10 ns region or shorter;
- the base spreading resistance of the bipolar transistor can be accurately controlled.

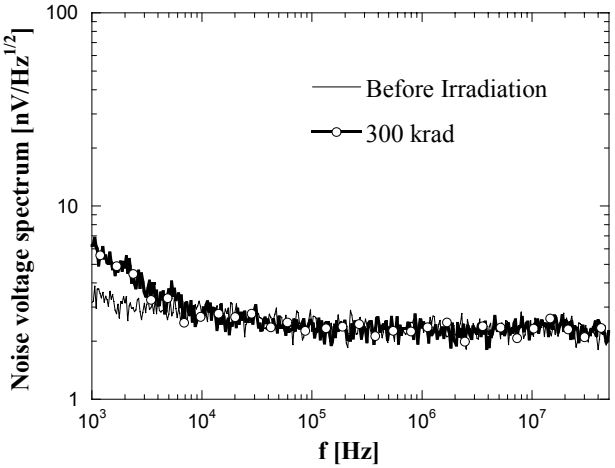

Fig. 16. Noise voltage spectra in an NPN bipolar transistor before and after exposure to ^{60}Co γ-rays. The device belongs to an SOI BiCMOS technology and it is biased at I_C = 500 μA and V_{CE} = 3 V.

The noise spectra of Fig. 16 [24], besides confirming the consideration about the effect of noise degradation due to the base spreading resistance, which brings the high frequency noise to about 2 nV/(Hz)$^{1/2}$ in a device which, according to theory should have 0.64 nV/(Hz)$^{1/2}$, shows an interesting point about noise in a bipolar transistor. The ordinary bipolar transistor is considered to be immune from 1/f-noise in the collector current. However, it has been demonstrated that if the device is exposed to radiation a 1/f noise component may appear. These considerations are confirmed by Fig. 16, which shows the noise voltage spectra in a bipolar transistor before and after irradiation.

Considering now the BiCMOS processes that feature a SiGe transistor as bipolar device, attention must be paid to the value of the base spreading resistance and to the 1/f noise in the base and collector current. In a charge measuring system a parallel noise component with a 1/f spectral density appears at the output of the charge-sensitive loop as a $1/f^3$ component after being integrated on the feedback capacitance. This spectral density would yield a divergent ENC contribution with a unipolar shaping. Which means that the use of SiGe transistor as a front-element requires an accurate control of the amount of the 1/f component in the base current noise and suitable attention in the design of the signal processor.

VI. Conclusions

The device scaling has addressed more favor toward the CMOS processes in the design of low-noise front-end systems for finely segmented radiation detectors. In particular, some limitations in their use that were related to their noise characteristics are gradually disappearing. Two aspects, however, need to be considered. One is the identification of the set of applications that may still require a different type of front-end device. The second one is related to the measures that are to be taken on order to improve the noise behavior of existing CMOS processes. Though consistently reduced, still the 1/f-noise sets the limit to the lowest achievable ENC. An essential requirement in this respect is that the quality of the gate oxide be maintained during when the thickness of the gate oxide is reduced. Finally, in applications involving peaking time in the nanosecond region the BiCMOS technologies may be a valuable solution, provided that efficient techniques to reduce the values of the base spreading resistance are adopted.

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